

Detector Support Group

We choose to do these things "not because they are easy, but because they are hard". Weekly Report, 2021-08-25

Summary

<u>Hall A – GEM</u>

Brian Eng, George Jacobs, Mindy Leffel, Tyler Lemon, Marc McMullen

• Installed six SBS gas flow sensor chassis in the Hall A gas distribution rack



Rear view of SBS gas distribution panel in Hall A

<u>Hall A – HV</u>

<u>Brian Eng</u>

• Developing Python script to generate grid of indicators for voltage differential (set – actual) which are colored based on alarm limits

<u>Hall A – SoLID</u>

Mary Ann Antonioli, Pablo Campero, Brian Eng, Mindy Leffel, Marc McMullen

- Completed drawings
 - * Axial Load Cells Measurement Wiring Diagram
 - * PLC IO, Remote A, Slot 8 Wiring Diagram
 - * Axial Load Cell Cable Diagram
- Updated *Cable List* spreadsheet
 - Added cable specifications required to connect voltage taps to quench detector units



<u>Hall B – RICH-II</u>

Mary Ann Antonioli, Peter Bonneau, Pablo Campero, Brian Eng, George Jacobs, Tyler Lemon, Marc McMullen

- Designed 4U tall chassis for hardware interlock system in NX12 to accommodate larger Backplane PCB
 - ★ Backplane PCB increased to 4" tall, creating less space for feedthroughs for chassis' power, network, USB connection, and gas system



New design for Hardware Interlock Chassis with larger Backplane PCB

• Updated N₂ purge system filter diagram



RICH II EEL N2 Purge Circuit Multi-Stage Filter Setup

Filter diagram for RICH-II N2 purge system



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<u>Hall C – NPS</u>

Mary Ann Antonioli, Peter Bonneau, Aaron Brown, Pablo Campero, Brian Eng, George Jacobs, Mindy Leffel, Tyler Lemon, Marc McMullen

- Generated, using Ansys, 36x30 matrix of PbWO₄ crystals surrounded by a 1.2 cm Cu shell; still need to add carbon fiber dividers between each crystal
 - ★ Preliminary analysis conducted using 0.5 W heat load applied to the rear face of each crystal
 - * Cu shell had a constant applied temperature of 10° C



Screenshot of thermal analysis done using 36x30 grid of PbWO₄ crystals – maximum temperature: 13.48°C

• Developing *Temperature Map* tab for LabVIEW Hardware Interlock Monitoring program

Crystal Zone Electr	onics	Zone	Chi	iller					
Main Front Temper	Back Temperatures			s Co	Cooling Circuit Temperatures			Temperature Map	
	Fr	ont Cry	stal Z	one Te	mpera	ture M	lap	~	
35	22.0	16.5	11.5	14.5	17.5	20.0	13.5		
4	19.5	14.0	18.5	24.0	12.0	16.5	18.5		
	18.0	14.5	14.0	17.0	21.5	15.0	17.5		
	16.5	24.0	21.5	22.0	17.0	16.5	20.5		
	22.0	20.5	19.5	20.5	20.0	23.0	20.5		
	14.0	21.5	20.5	22.0	15.0	24.0	17.5		
	23.0	18.0	25.0	17.5	24.0	24.0	15.0		
	20.0	17.5	16.5	14.5	17.0	17.5	16.0		
0							1044		

Screenshot of Temperature Map tab from Hardware Interlock Monitoring LabVIEW program

EIC

<u>Brian Eng</u>

• Silicon tracker model now using DC-DC converter to cut down on cable service size (thinner cables)